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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Ramesh V. Peri	§	Art Unit:	2186
Serial No.:	10/717,085	§	Examiner:	Paul W. Schlie
Filed:	November 19, 2003	§	Atty Docket:	ITL.1059US (P17918)
For:	Accessing Data from Different Memory Locations in the Same Cycle	§	Assignee:	Intel Corporation

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Commissioner for Patents
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REPLY BRIEF

This reply brief responds to the new issues raised by the Examiner. In particular, the Examiner's previous reliance on the Kawasaki reference as teaching simultaneous writes is apparently withdrawn. Thus, it is necessary to address additional issues.

The Kawasaki patent relates to a multiple port cache memory 1. It can be accessed through ports A and B (see e.g., Figure 7). The alleged invention is to use less bits than 30 (i.e. 6) to determine whether the same address is being accessed at both ports. The prior art uses all 30 bits to determine if there is a simultaneous access to the same address.

The problem is that the reference never really says what happens if there is a simultaneous access because the goal of the patent is detection, not access. (See e.g., newly cited claim 1 of the reference and column 2, lines 15-18 and column 1, lines 10-17).

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I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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The only logical conclusion is that the exact same address cannot be accessed simultaneously. Therefore, the point of detection is not to futilely simultaneously access the same address, but, rather, to accommodate for this anomalous situation. This conclusion is suggested by the reference which indicates that when simultaneous storage commands are received, one will be necessarily (and logically) executed before the other. (See column 1, lines 58-62).

The assertion on page 3, lines 11-13 of the Answer that one or more of the multiple ports may be selected simultaneously is unsupported by the cited material. The cited material refers neither to words or multiple words or what to do in the case of multiple accesses to the same address, other than to detect such a situation.

The mention of additional references, including Johnson, never cited during prosecution, is insufficient at this late date and too incompletely explained to fashion a belated Section 103 rejection.

Any asserted Section 103 rejection fails to make out a *prima facie* rejection because the basis for such a rejection is never set out nor is any rationale to combine or modify, based on cited art, ever set out.

Therefore, the rejection should be reversed.

Respectfully submitted,

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